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O. Bourrion, L. Gallin-Martel

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An integrated CMOS Time-to-Digital Converter for coincidence detection in a Liquid Xenon PET prototype

Olivier Bourrion, Laurent Gallin-Martel*

Laboratoire de Physique Subatomique et de Cosmologie, 53 avenue des Martyrs 38026 Grenoble France

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Abstract

A Time to Digital Converter was designed (CMOS 0.35 µm) to perform coincidence detection in a Liquid Xenon PET prototype. This circuit proved to be able to operate at 150 K, while showing a resolution better than 250 ps. The circuit enables a low readout dead time (<90 ns) and provides a fully synchronous digital interface for easy data retrieval.

Keywords: Delay locked loop (DLL), time to digital converter (TDC), positron emission tomography (PET)
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1. Introduction

A R&D project based on the use of Liquid Xenon (LXe) for small animal Positron Emission Tomography (PET) was initiated in 2001 [1]. The LXe combines high light efficiency and fast response. Prototype modules dedicated to γ photons detection are under study (fig.1).

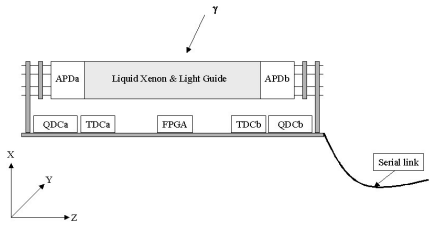

Fig. 1. LXe prototype module

* Corresponding author. Tel.: +33-4-76-28-40-84; fax: +33-4-76-28-40-04; e-mail: laurent.gallin-martel@lpsc.in2p3.fr.

On the contrary of crystal based detectors, these modules are aimed to be distributed axially of the field of view allowing the Depth Of Interaction (DOI) measurement. The self triggered front end electronics has to be located close to the photo detectors (multi anodes photomultiplier tube or avalanche photodiode array) and to operate at 165 K. This electronics performs charge measurement for each pixel (QDCn) and time tagging for each event (TDCn). The module is controlled by a FPGA that performs (x, y, z) coordinates on line calculation and serial link management.

2. Design of the TDC

2.1. Background

The aim of this project was not to design a very high resolution TDC (see [2] for the different kinds of TDC), but a functional one for a LXe PET application. This implies that the chip must operate at 165 K with a resolution better than 1 ns. The power consumption, and the dead time have to be kept at minimum values. All these criteria lead to the choice of a TDC based on a Delay Locked Loop (Fig. 2).

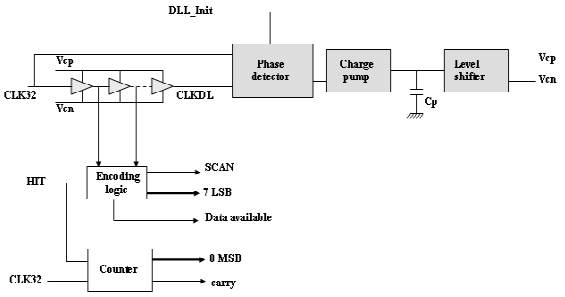

Fig. 2. TDC block diagram

The TDC comprises a 128 delay cell chain that is fed by a reference clock (CLK32). On a HIT signal occurrence the state of the chain is registered. The HIT signal delay within the present CLK32 cycle can be deduced from the CLK32 rising edge location in the delay chain. This position is then encoded to provide the delay fine value. Only one CLK32 rising edge must be propagated in the chain to ensure proper encoding. The chain is included in a Delay Locked Loop (DLL) which enables continuous self calibration of the TDC and ensures the long term stability by reducing the process and temperature dependencies. The delay coarse measurement is provided by an 8 bit counter and allows the event to be associated to the right CLK32 cycle. The Data Available signal ensures synchronous data retrieval. The state of the delay chain can also be outputted (SCAN output) in test mode.

2.2. Delay Locked Loop

As shown in Fig.2, the DLL is composed of 128 elementary delays, a phase detector, a charge pump and a level shifter.

2.2.1. Elementary delay cell

This cell comprises 2 starved inverters controlled by Vcp and Vcn signals and ensures a 244 ps resolution (128 cells fed by a 32 MHz clock) over the process best and worst cases.

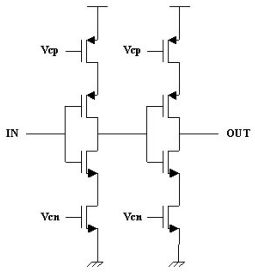

Fig. 3. Voltage controlled delay element

This architecture is not the best one for fine resolution point of view, but since this cell is highly symmetric a very good clock duty cycle conservation is achieved allowing long delay chain implementation without additional constraint on Vcp and Vcn signals. Other configurations have been used [3] [4] requiring special cares to match the delay of the rising and falling edges.

2.2.2. Phase detector

The phase detector provides a phase difference information for performing the delay line regulation (Fig. 4.). With such an implementation (so-called bang-bang configuration), the line full scale delay is oscillating around the value of the one clock period. This leads to the intrinsic jitter of the DLL. Other

kinds of phase detector have been designed but they exhibit other drawbacks [5]. The implementation of this block has to be symmetrical otherwise an offset phase is induced.

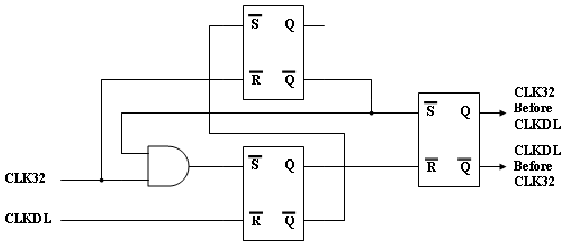

Fig. 4. Bang-bang phase detector

2.2.3. Charge pump and level shifter

The charge pump is fed with the signal provided by the phase detector for charging/discharging an external capacitor during one clock cycle (Fig.5).

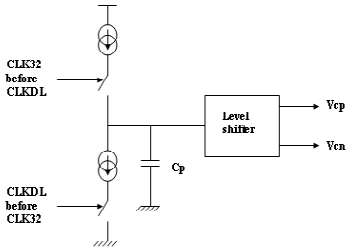

Fig. 5. Charge pump and level

The voltage increment/decrement has to be as small as possible to limit the DLL jitter. The capacitor voltage is processed by the level shifter that generates the control voltages Vcp and Vcn. This shifter also performs the linearization of the function delay=f(Vcp,Vcn) [2].

2.3. Line memorization

A buffer is inserted between the delay line and the D register in order to restore the signal slew rate. The probability to observe a metastable cell is leveled down and a proper line memorization can be achieved. This function was implemented as a part of the delay cell itself and duplicated 128 times to ensure a good differential non linearity (Fig. 6.). The clock tree distributed to the memorization cells has to be perfectly balanced as well.

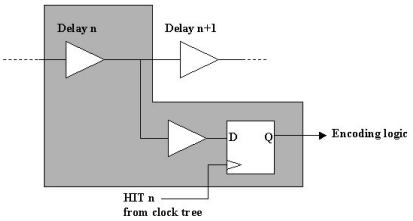

Fig. 6. Delay line memorization

2.4. Digital part architecture

The HIT signal is gated by a latch which does not allow a new trigger as long as the previous data has not been treated (Fig.7).

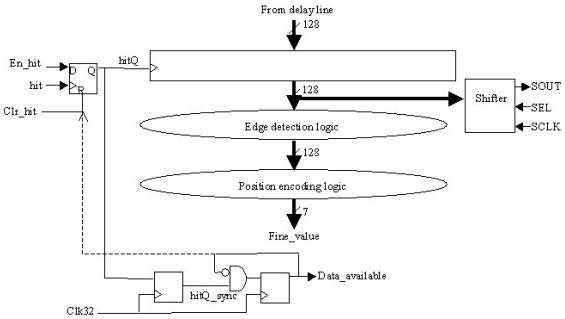

Fig. 7. Digital part overview

The accepted trigger is resynchronized through two consecutive latches for generating a data available flag and thus providing an easy readout interface. This induces a dead time lower than 3 CLK32 cycles.

2.4.1. Position encoding methodology

Two steps are needed to generate an encoded value of the delay line state. At first, the clock rising edge must be localized in the memorized delay line, and then the corresponding code must be provided.

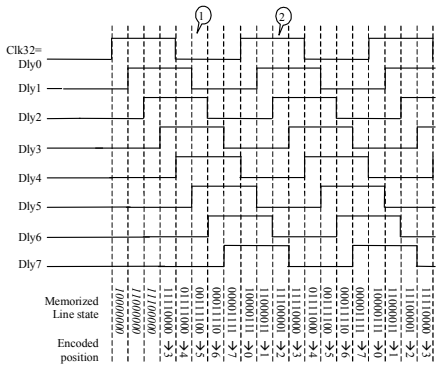

Fig. 8. Eight cell delay line timing

If a close look is taken at the state of an eight element delay line (Fig.8), we can see that the fine delay is determined by the number of the last bit at 1 before the 1 to 0 transition in the memorized line state. For instance when hit #1 occurs, the only delay element having its signal rising is Dly5, and the corresponding code (01111000) yields bit 5. The digital system that allows detecting this edge in a line is given below Fig.9 (duplicated 128 times), it also provides a safety against defect in the memorized line due to metastability.

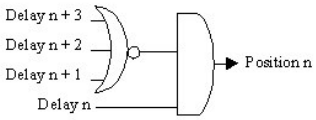

Fig. 9. Edge detection logic

Once the edge is located (only one bit at a time in the line), the position has to be encoded. It can be easily done with OR gates. Below is given the methodology for an 8 bit line.

Pos X	Bit 2	Bit 1	Bit 0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

One can notice the following:

- Bit0 = Pos1 or Pos3 or Pos 5or Pos 7;
- Bit1 = Pos2 or Pos3 or Pos6 or Pos7;
- Bit2 = Pos4 or Pos5 or Pos6 or Pos7;

This can be easily extended for a 128 bit line.

2.4.2. Coarse counting

Once the HIT has been encoded at a resolution of 244 ps, it must still be associated with the proper clock cycle. For doing that the architecture proposed by C. Lujslin [3] was used, where 2 counters are counting, one on the rising edge of the clock and the other one on the falling edge (Fig.10). Then, when a HIT occurs, both counter values are registered and the relevant one (stable at the sampling time) is multiplexed to the output. The multiplexer is controlled by the MSB of the fine value. A carry output is provided for counter range extension.

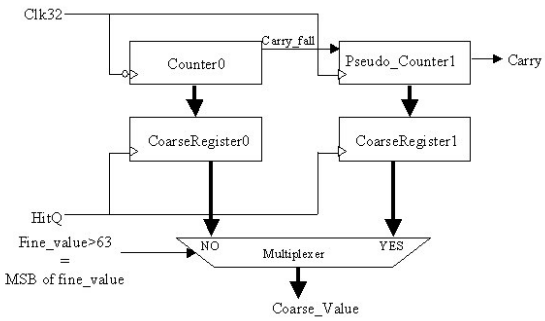

Fig. 10. Coarse counting architecture

3. Chip test results

5 chips were packaged and tested.

- Resolution: 244 ps with a clock at 32 MHz
- DLL lock range: from 20 MHz to 40 MHz
- Differential non linearity: +/-20% (0.2 LSB) (excepted for channel 126 and 127, due to a layout problem)
- Integral non linearity: <1%
- Jitter: <35 ps (at the output of the 128th delay cell)
- Line state serial monitoring is functional
- Consumption: 14mW

Testing in the cryostat showed that the TDC can operate least to 150 K.

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